REMARKS/ARGUMENTS

In the Office action dated July 23, 2003, the Examiner rejected claims 1 and 11 under 35 U.S. C. § 102(b) as being anticipated by U.S. Patent No. 4,703,551 to Szluk *et al.* Claims 6, 10 15-17 and 22 stand rejected under 35 U.S. C. § 102(b) as being anticipated by U.S. Patent No. 5,757,045 to Tsai *et al.* Claims 2-4 and 12-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over '551 in view of U.S. Patent No. 6,069,044 to Wu. Claim 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over '551 in view of '045. Claims 7-9 and 18-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over '045 in view of '044. The Examiner stated, on page 6 of the Office action, that claims containing the limitation "single mask, single step implantation" were not limited to a single mask and single step process. This contention is addresses later in this Preliminary Amendment.

In the Specification, no changes.

In the Claims, Claims 1-4, 7-9, 11 and 13-15 are currently amended; claims 6 and 17 were previously amended; claim 21 remains cancelled. The remaining claims are as originally filed.

The Invention

The invention is a method of forming a MOS or CMOS device on a silicon substrate. The substrate is prepared, and includes a conductive region of a first type, such as an n-type or p-type conductive region, which has a first device active area therein. Two such regions are prepared, of opposite conductive types, for a CMOS device. A gate electrode is formed on the active area(s). Ions of an opposite conductivity type to that of the conductive region of the first type are implanted into the conductive region of the first type to form a source region and a drain

region on opposite sides of the gate electrode. An important feature of the invention is the fabrication of a device using only a single implantation step and a single mask and the deposition of a silicide layer by selective CVD, which does not require further masking, and which does not, by virtue of the deposition of silicide, as opposed to deposition of a metal and formation of a silicide, or deposition of a silicide layer on as silicon substrate, does not reduce the thickness of the silicon substrate or component. The reduction in implantation and masking steps saves time and reduces the overall cost of the fabrication process. In fact, the method of the invention saves two mask levels during fabrication of a CMOS device, and saves two-ion implantation steps during CMOS fabrication. The silicide layer is formed with only a single, selective CVD process.

The Applied Art

U. S. Patent No. 4,703,551 to Szluk *et al.* describes a method of implantation which requires at least two, and likely three, separate implantation steps. Not only are these multiple implantation steps described in the Specification, the claims of '551 require multiple implantation steps. Elimination of any of the doping steps will render any devices formed by the method of the invention inoperative. One implantation step is described as lightly doping, col. 9, lines 30-50, while another implantation step is described as heavy doping, col. 5, line 66 - col. 6, lines 14. If the light doping step is conducted with too great an ion dose, the ions will leak into the channel, rendering the device inoperative. Thus, multi-step masking and implantation steps are required by the '551 reference. A tungsten layer is formed, and is stated to be equivalent to a refractory metal silicide layer. Col. 9, lines 61- col. 10, line 7. However, additional masking is required for this process, and regardless of whether the deposition is metal and a silicide conversion, or a silicide deposition, both take place on a silicon substrate, and will, during subsequent annealing, will

reduce the thickness of the silicon substrate.

U. S. Patent No. 5,757,045 to Tsai *et al.* describes a standard silicide process, and also describes, and requires, multiple masking and implantation steps for active area formation in the CMOS. Col. 3, line 65 to col. 5, line 22.

U. S. Patent No. 6,069,044 to Wu describes a multi-step, low energy implantation process.

The Claims

All of the independent claims require that the implant of the second type ions be accomplished using a single mask and in a single implant step. The Examiner's argument that the claims are not so limited (Office action, page 6) because of the standard claim construction use of "comprising" is not correct: while other steps could be, and are most certainly used, to construct a usable, marketable device, the language of the claims is quite clear and only subject to a single legal interpretation that any and all implantation of second type ions must be accomplished using a single mask and in a single step. If the Examiner continues to disagree with Applicants' position, the Examiner is invited to suggest language which will meet this limitation.

The Examiner states that '551 "apparently teaches a solo implantation step to form source/drain regions 28N." However, a close reading of '551 reveals that three separate masking and implantation steps are required to form the three requisite active areas 28N, 32N and 34N: these structures are formed using the steps as described in col. 6, line 38, through col. 8, line 38. '551 doesn't form any active area in a single mask, single implant step. Likewise, '045 does not teach or suggest single mask, single step ion implantation as taught and claimed by Applicants. All of the independent claims stand rejected under 35 U.S. C. § 102, yet the Examiner goes beyond the

teachings of the applied references to provide a reasons for rejecting the claims under 35 U.S. C. § 102, which is akin to a 35 U.S.C. § 103(a) rejection, however, as the rejection is under 35 U.S. C. § 102, Applicants must respond to the rejection as stated. Applicants teach the formation of a MOS or CMOS device using a single mask and single step ion implantation for second type ions - they do not go beyond the scope of the recited language. The Examiner has broadened Applicants' claims, and then rejected them based on art which uses multiple masks and implantation steps. Such is not a proper 35 U.S. C. § 102 rejection.

Claim 1 is currently amended to recite that the implanting ions step [second type] uses a single mask and requires only a single implantation step. '551 is applied as a 35 U.S. C. § 102 reference, however, '551 requires a first mask and implantation step, col. 6, line 38 to col. 7, line 51, and a second mask and implant step, col 7, lines 52-68. Silicide, vice a metal, as preferred by '551 is deposited using the same mask over the source, drain and gate. Regardless of whether '551 uses a metal converted to silicide or a direct silicide deposition, the prescribed masking allows the metal or silicide to overlay silicon, which will result in a decrease in silicon thickness as the silicide is formed, or as subsequent annealing of the structure causes the deposited silicide to eat into the silicon. Applicants' invention does not allow the silicide to contact silicon, as the silicide is selectively CVDd over the source, drain and gate - not the underlying silicon as is done by '551, thus leaving the silicon at its desired, required thickness. It will be recognized by one of ordinary skill in the art that modifying '551 according to Applicants' teaching, as has been done by the Examiner, renders the device of '551 inoperative. Amended claim 1 is allowable over the applied prior art.

Claim 2 has been amended to recite that the result of the single step implant is a

shallow implant. The combination of '551 and '044, if it is at all possible to combine these two references into an operable device, suggest a deep implant. It really is not possible to combine the references, however, because the energies and doses do not overlap, thus using the energy and dose of '044 with '551 will not produce a usable device: '551 requires, col. 7, lines 60-68, an energy of 80 keV at an ion dose of $5x10^{15}$ to $5x10^{16}$ cm^{-2}; '0441 requires, col. 4, lines 57-60, an energy of .3 keV to 5 keV at an ion dose of $1x10^{13}$ to $1x10^{15}$ cm^{-2}. So, while '044 may suggest an energy and dose close to that taught by Applicant, the use of such a dose in the invention of '551 will not produce the high energy, deep implant required by '551. Claim 2 is allowable over the applied art.

Claim 3 has been amended to recite that the result of the single step implant is a MDD device. Specification, page 7, lines 1-8. As previously noted, it is not possible to combine the '551 and '044 references because the energies and doses do not overlap, thus using the energy and dose of '044 with '551 will not produce a usable device: '551 requires, col. 7, lines 60-68, an energy of 80 keV at an ion dose of $5x10^{15}$ to $5x10^{16}$ cm^{-2}; '0441 requires, col. 4, lines 57-60, an energy of .3 keV to 5 keV at an ion dose of $1x10^{13}$ to $1x10^{15}$ cm^{-2}. So, while '044 may suggest an energy and dose close to that taught by Applicant, the use of such a dose in the invention of '551 will not produce the high energy, deep implant required by '551. Claim 3 is allowable over the applied art.

Claim 4 is a combination of claims 2 and 3 with the result stated in a concentration format. Claim 4 is allowable for the reasons set forth in connection with claims 2 and 3.

Claim 5 is allowable with its allowable parent claim.

Claim 6 was previously amended to emphasize that the implantation for a MOS device is done in a single step with a single mask, and that the deposition of silicide is done

selectively. This differs from the teachings of the applied references, taken separately or alone. In the pending Office action, the Examiner did not cite any portion of the applied references to the element of the single mask, single step implantation. The Examiner's contention that the claims is not limited to the claim language has been previously disposed of. Claim 6 is allowable over the prior art of record.

Claims 7-9 are allowable for the reasons set forth in connection with claims 2-4.

Claim 10 is allowable with its allowable parent claim.

Claim 11 is currently amended to include the single mask, single step implantation limitation. Claim 11 is allowable as filed because the applied reference requires multiple masking and implantation steps, and the devices constructed according to the references will be inoperative with only a single implantation step.

Claim 12-14 are allowable for the reasons set forth in connection with claims 2-4.

Claim 15 has been amended to recite that the selective CVD of silicide occurs only over source, drain and gate regions and not over any underlying silicon. Claim 15 is allowable because the applied reference teaches application of a metal or a silicide over both active areas and over exposed silicon. As previously discussed, such action will ultimately reduce the thickness of silicon where the metal or silicide is applied, resulting in degradation of device performance.

Claim 16 is allowable with its allowable parent claim.

Claim 17 was previously amended to include the single mask, single implant step, which was not addressed by the Examiner in the current office action. This claim is allowable for the reasons set forth in connection with claims 1 and 11. Claim 17 is allowable as amended because the applied art requires multiple implantation and masking steps.

Claims 18-20 are allowable for the reasons set forth in connection with claims 2-4.

Claim 22 is allowable with its allowable parent claim.

In light of the foregoing amendment and remarks, the Examiner is respectfully requested to reconsider the rejections and objections state in the Office action, and pass the application to allowance. If the Examiner has any questions regarding the amendment or remarks, the Examiner is invited to contact the undersigned.

Provisional Request for Extension of time in Which to Respond

Should this response be deemed to be untimely, Applicants hereby request an extension of time under 37 C.F.R. § 1.136. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any over-payment to Account No. 19-1457.

Respectfully submitted,

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